

XXIII internationale beroepen wedstrijden utrecht 1977

E L E C T R O N I C N B. 16

Resumen de Calificaciones

INTERNATIONAL VOCATIONAL TRAINING COMPETITIONS
CONCURSO INTERNACIONAL DE FORMACION PROFESIONAL

Trade : Electronic Ind. No. 16
Especialidad _____

Marking concepts Conceptos de calificación		Maximum marks puntos	Marks of individual contestants/Calificación individual de los concursantes									
			No. 1	No. 2	No. 3	No. 4	No. 5	No. 6	No. 7	No. 8	No.	No.
A	Drawing: circuit diagramm	10	8	7	6	8	9	9	8	8		
B	Drawing of a printed circuit	10	8	3	0	2	6	10	1	1.5		
C	Calculation (20 problems)	20	13.9	12.7	11.8	12.3	10	19.8	16.8	16.5		
D	Practical Project "Timer"	60	44	51.5	41	40.5	44.5	50.5	37	51.5		
Included in the practical portion												
Quality/Calidad - Marks/Puntos												
T Time marks/Por tiempo puntos												
Total Marks/Puntos		100	73.9	74.2	58.8	62.8	69.5	89.3	62.8	77.5		
_____ a _____ Place/Puesto			3	3	8	6	5	1	6	2		
de 8.7 de 1977 Price/Premio												
Certified/Certifico El Secretario General		Countries Países	Germany Alemania	Corea	España	USA	Holland	Japan	UK Reino Unido	Schweiz Suiza		

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INTERNATIONAL VOCATIONAL TRAINING COMPETITIONS
CONCURSO INTERNACIONAL DE FORMACION PROFESIONAL

MARKING RESULTS
CALIFICACION

Trade : Electronic No. 16
Especialidad

Contest. Concur- sante No.	Surname Apellidos	Christian name Nombre	Nationality Nacionalidad	Points Puntos
1	Hecht	Walter	Alemania	73.9
2	KIM	Sae Hwan	Corea	74.2
3	Marquinez Lopez de Erenchun	Feliciano	España	58.8
4	Curd	Steve E	USA	62.8
5	Zuur	J. D.	Holanda	69.5
6	Andou	Yasuhiro	Japon	89.3
7	Donnelly	David Robert	Reino Unido	62.8
8	Marti	Kurt	Suiza	77.5
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				

PROPOSED PRICE LIST
PROPUESTA DE PREMIOS

Prices Premios	Contest. Concur- sante No.	Surname Apellidos	Christian names Nombre
1	6	Andou	Yasuhiro
2	8	Marti	Kurt
3	2	Kim	Sae Hwan
3	1	Hecht	Walter

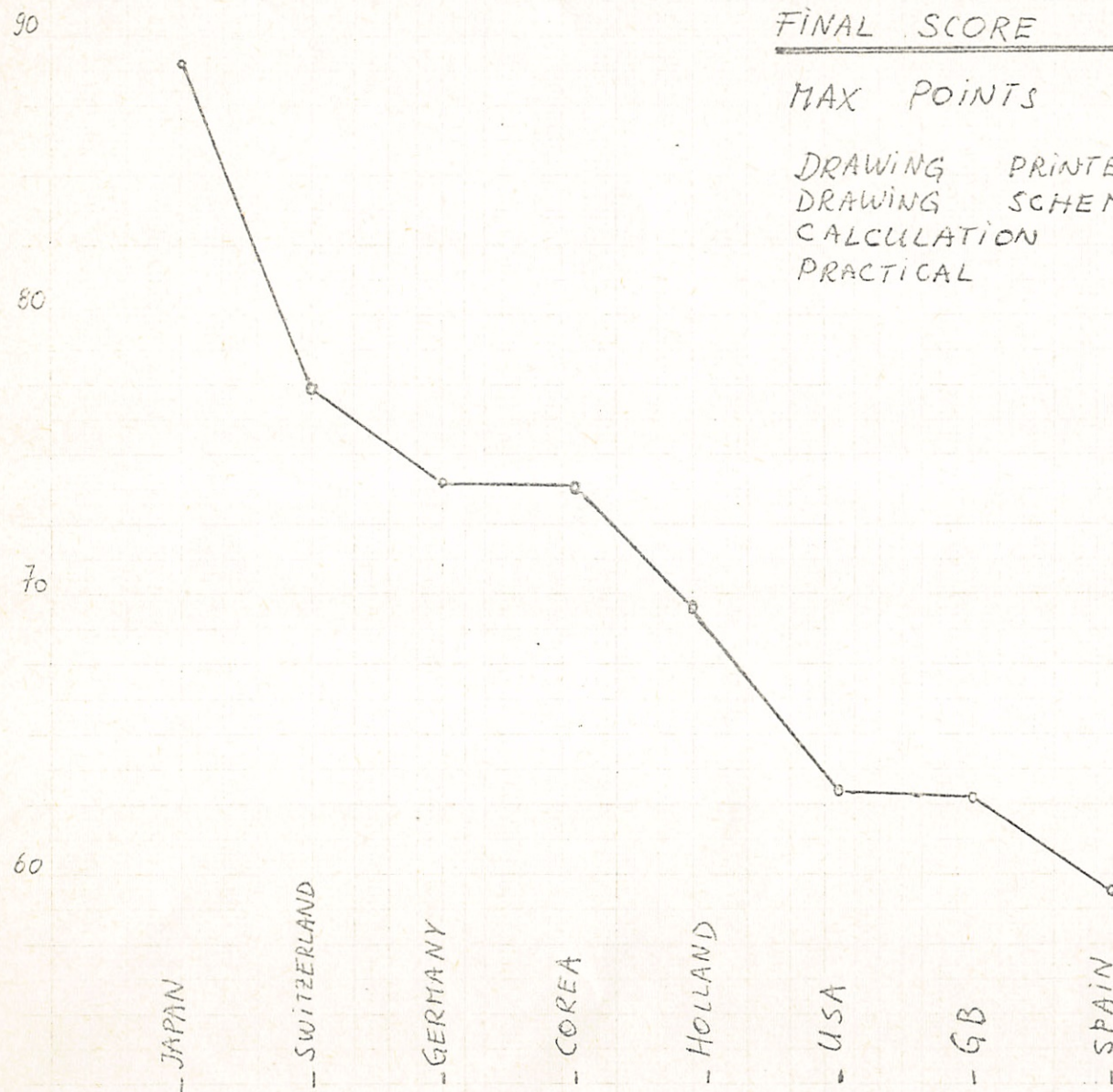
President of marking jury Lin cheng chun Technical expert
El Presidente del jurado Expertos técnicos:

President of Technical Committee
El Presidente del Comité Técnico :

FINAL SCORE ELECTRONIC

MAX POINTS 100

DRAWING	PRINTED CIRCUIT	10
DRAWING	SCHEMA	10
CALCULATION		20
PRACTICAL		60

100.

8.7. 1977

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INTERNATIONAL VOCATIONAL TRAINING COMPETITIONS
CONCURSO INTERNACIONAL DE FORMACION PROFESIONAL

16

Language : English
Idioma : _____

MARKING CRITERIA
CRITERIOS DE CALIFICACION

Plan No. _____
Plano

Trade Electronic No. 16
Especialidad

Concepts Conceptos	Designation of concepts Denominación de los conceptos	Maximum marks Puntos máximos	Remarks Observaciones
A	Drawing of a circuit diagram	10	1½ hour
B	Drawing of a printed circuit	10	1½ hour
C	Calculation (20 problems)	20	4 hours
D	Practical Project Electronic Timer	60	12 hours
E			
F			
G			
H			
I			
J			
K			
L			
M			
N			
O			
P			
R			
TIME TIEMPO			19 hours
	TOTAL MARKS PUNTOS	100	

UTRECHT 1977

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Resumen de Calificaciones

INTERNATIONAL VOCATIONAL TRAINING COMPETITIONS
CONCURSO INTERNACIONAL DE FORMACION PROFESIONAL

Trade : Electronic No. 16
Especialidad _____

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PRACTICAL

Marking Summary

Resumen de Calificaciones

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INTERNATIONAL VOCATIONAL TRAINING COMPETITIONS

Trade

: Electronic

No. 16

CONCURSO INTERNACIONAL DE FORMACION PROFESIONAL

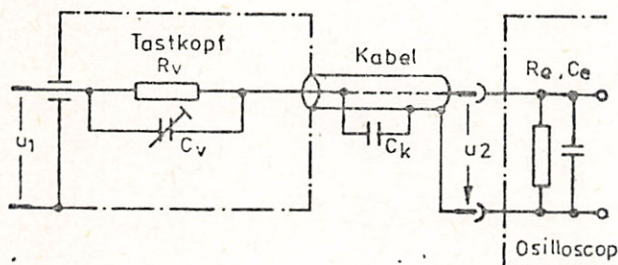
Especialidad

Marking concepts Conceptos de calificación	Maximum marks puntos	Marks of individual contestants/Calificación individual de los concursantes									
		No. 1	No. 2	No. 3	No. 4	No. 5	No. 6	No. 7	No. 8	No.	No.
Electrical function	16	16	16	16	16	16	16	16	16		
Number of jump	5	0	3.5	4	2.5	2.5	4.5	3	5		
Quality of soldering	8	1.5	1.5	2.5	6	6.5	5	7	8		
" of harness	4	1.5	2.5	0.5	2	3.5	1	4	3		
Switch rotation sequence	1	1	1	1	1	1	1	1	1		
Switch position	1	1	1	1	1	1	1	1	1		
Serviceability	5	1	4	3	2	4	2	5	3		
General aspect	5	1.5	2	0.5	4	3	1	3.5	2.5		
Work method organization	2	2	1	2	2	2	2	2	2		
Mechanical integrity	3	1.5	0.5	1	1.5	3	1	2	3		
Broken (damaged) components	5	5	5	5	5	5	5	5	3		
Quality/Calidad - Marks/Puntos											
T Time marks/Por tiempo puntos	5	5	3	4	1	3	5	2	4		
Total Marks/Puntos	60	37	41	40.5	44	50.5	44.5	51.5	51.5		
_____ a _____ Place/Puesto											
de _____ de 19 _____ Price/Premio											
Certified/Certifico El Secretario General	Countries Países	GB	SPAIN	USA	Germany	Japan	Holland	Schweiz	Corea		

Aufgabe 4:

Ein Breitbandoszilloskop hat eine Eingangsimpedanz von $R_e = 1 \text{ M}\Omega \parallel C_e = 36 \text{ pF}$. Es soll ein Breitbandspannungsteiler mit einer Teilung von $20 : 1$ entworfen werden. Das Verbindungskabel (Kapazität 30 pF/m) soll $1,20 \text{ m}$ lang sein.

Berechnen Sie die Werte für die Bauteile R_v und C_v und tragen Sie die Ergebnisse in die Skizze ein.



Lösung:

$$R_v = (n-1) \cdot R_e = 19 \cdot 1 \text{ M}\Omega = \underline{19 \text{ M}\Omega};$$

$$C_k = 1,2 \text{ m} \cdot 30 \text{ pF/m} = 36 \text{ pF};$$

$$C_e' = C_e + C_k = 36 \text{ pF} + 36 \text{ pF} = 72 \text{ pF};$$

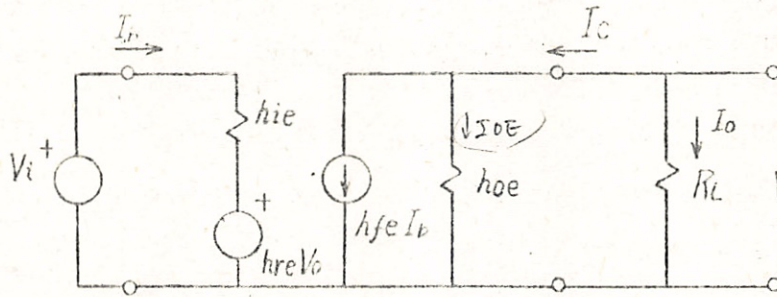
$$\frac{C_v}{C_e'} = \frac{R_e}{R_v} \rightarrow C_v = C_e' \frac{R_e}{R_v}$$

$$\underline{C_v} = 72 \text{ pF} \cdot \frac{1 \text{ M}\Omega}{19 \text{ M}\Omega} = \frac{72 \text{ pF}}{19} \approx \underline{3,8 \text{ pF}}$$

PROPOSAL OF THE TECHNICAL REPRESENTATION OF GERMANY

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15. The transistor has the following h -parameters: $h_{ie}=2500\Omega$, $h_{re}=4 \times 10^{-4}$, $h_{fe}=50$, and $h_{oe}=10\mu S$ as show in the figure below For $R_L=5k\Omega$ and $I_0=0.2mA$ rms, estimate the current gain and voltage gain of the amplifier.



図のトランジスタは $h_{ie}=2500\Omega$, $h_{re}=4 \times 10^{-4}$, $h_{fe}=50$, $h_{oe}=10\mu S$ である。

$R_L=5k\Omega$, $I_0=0.2mA$ (実効値) である
増幅量の電流増幅度、電圧増幅度 V_0^+ を求めよ。

$$\begin{aligned} V_0 &= I_0 R_L \\ &= 0.2 \times 5 \\ &= 1 [V] \end{aligned}$$

$$A_i : -47$$

$$\begin{aligned} I_2 &= I_0 + I_{oe} & I_{oe} &= V_0 h_{oe} \\ &= 0.2 + 0.01 & &= 1 \times 10^{-4} \\ &= 0.21 [mA] & &= 10 \mu A \end{aligned}$$

$$A_v : -95$$

$$\begin{aligned} I_B &= \frac{I_2}{h_{fe}} & V_1 &= I_B h_{ie} + V_0 h_{oe} \\ &= \frac{0.21}{50} & &= 4.2 \times 10^{-3} \times 2500 + 1 \times 10^{-4} \\ &= 4.2 \times 10^{-3} & &= 10.5 + 0.01 \\ & & &= 10.51 [mV] \end{aligned}$$

$$\begin{aligned} A_v &= \frac{V_0}{V_1} \\ &= \frac{1}{10.51} \times 10^3 \\ &= 95.14 \end{aligned}$$

$$\begin{aligned} A_i &= \frac{I_0}{I_B} \\ &= \frac{0.2}{4.2 \times 10^{-3}} \\ &= 47.61 \end{aligned}$$

Aufgabe 10 :

Für eine Zwischenfrequenz von $f_z = 468 \text{ KHz}$ ist ein Sperrkreis zu dimensionieren. Es steht eine Spule mit einer Induktivität von $L = 578 \mu\text{H}$ zur Verfügung.

Welche Kapazität muß der Spule parallel geschaltet werden

Geg.: $f_z = 468 \text{ KHz}$; $L = 578 \mu\text{H}$;

Ges.: C

Lösung:

$$f_z = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \Rightarrow C = \frac{1}{\omega^2 \cdot L} = \frac{1}{6,28^2 \cdot 4,68^2 \cdot 10^{10} \cdot 5,78 \cdot 10^{-4}}$$

$$= \frac{1}{39,438 \cdot 21,9 \cdot 5,78 \cdot 10^6} = \frac{1000 \cdot 10^{-9}}{510 \cdot 10^3} =$$

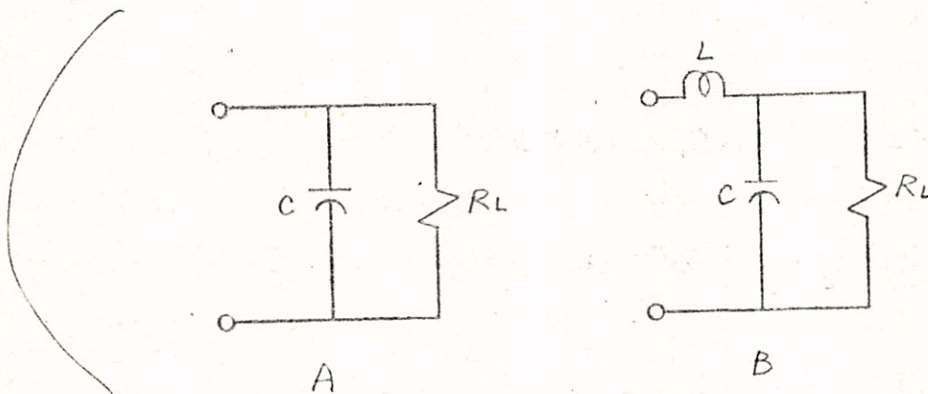
$$= 0,2 \cdot 10^{-9} \text{ F,}$$

$$\underline{\underline{C = 200 \text{ pF,}}}$$

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13. Filters A and B are both designed to provide 2% ripple factors when operated with 60-Hz rectifiers. Predict the new ripple factors if the input frequency is increased to 120Hz, with all other factors unchanged.



○ フィルタ A と B は 60Hz を電流している時リップル率は 2% に設計されている。他の定数は変えずに周波数を 120Hz に増加した時のリップル率を求めよ。

$$A. \quad r = \frac{1}{2\sqrt{3} C R f}$$

$$2\sqrt{3} C R = \frac{1}{r f}$$

$$r' = \frac{1}{2\sqrt{3} C R f'}$$

$$= \frac{1}{\frac{1}{r f} f'}$$

$$= \frac{r f}{f'}$$

$$= \frac{2 \times 60}{120}$$

$$= 1 (\%)$$

$$B. \quad r = \frac{\sqrt{2}/3}{4\omega^2 L C}$$

$$\frac{\sqrt{2}}{12(2\pi)^2 L C} = f^2 r$$

$$r' = \frac{\sqrt{2}}{12(2\pi)^2 L C f'^2}$$

$$= \frac{r f^2}{f'^2}$$

$$= \frac{2 \times 60^2}{120^2}$$

$$= \frac{2}{4}$$

$$= 0.5 (\%)$$

A

1 [%]

B

0.5 [%]

5. A load connected across a 200-V, 60Hz line draws 20kW at a leading pf of 0.5.

~~(a) Calculate the current and the reactive power.~~

Q (a) What series combination of circuit elements is equivalent to this load?

Q (b) What parallel combination of circuit elements is equivalent to this load?

進み力率 0.5 20kWで 200V 60Hzの電線につなかれた負荷があります

(a) 電流・無効電力を求めよ

(b) この負荷と等価で直列構成の回路の要素は何か

(c) この負荷と等価で並列構成の回路の要素は何か。

(a) $P = VI \cos \theta$

$$I = \frac{P}{V \cos \theta}$$

$$= \frac{20k}{200 \times 0.5}$$

$$= 200 [A]$$

$$P_{var} = \sqrt{40^2 - 20^2}$$

$$= \sqrt{1200}$$

$$= 34.64 \text{ kVar}$$

$$R = \frac{V}{I}$$

$$= \frac{200}{100}$$

$$= 2 [\Omega]$$

$$X_C = \frac{200}{173}$$

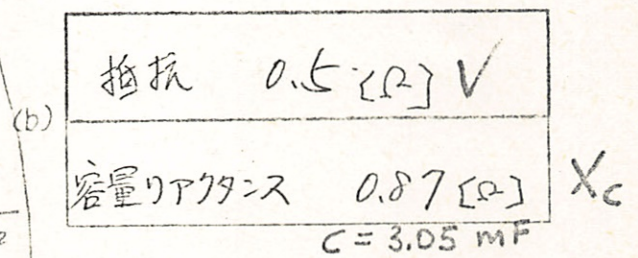
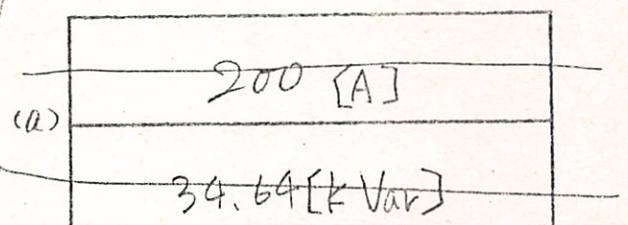
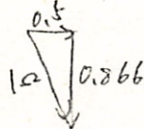
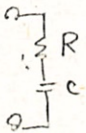
$$= 1.154 [\Omega]$$

(b) $Z = \frac{V}{I}$

$$= \frac{200}{200}$$

$$= 1 \Omega$$

$$Z = 0.5 - j0.866$$



(c) $I_R = 200 \cos \theta$

$$= 200 \times 0.5$$

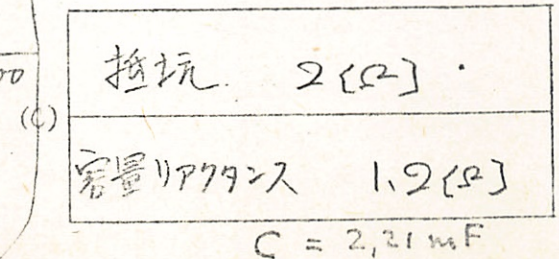
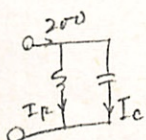
$$= 100 [A]$$

$$I_C = \sqrt{200^2 - 100^2}$$

$$= \sqrt{40000 - 10000}$$

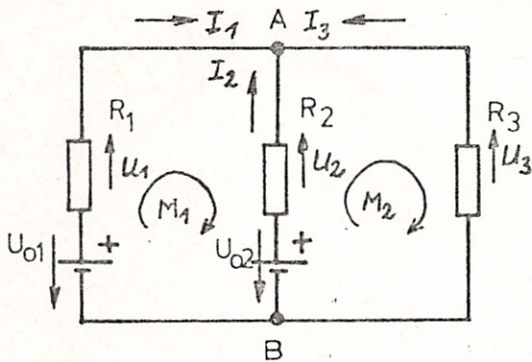
$$= \sqrt{30000}$$

$$= 173 [A]$$



Aufgabe 2 :

Für das vorgegebene Netzwerk sind die Spannungsabfälle an den Widerständen R_1 , R_2 und R_3 zu berechnen.



Gegeben: $U_{01} = 10 \text{ V}$; $U_{02} = 5 \text{ V}$;

$R_1 = 1 \text{ k}\Omega$; $R_2 = 2 \text{ k}\Omega$;

$R_3 = 5,6 \text{ k}\Omega$;

Gesucht: U_1, U_2, U_3

Lösung:

Zur Unterscheidung von den techn. Strömen werden die Maschenströme als i_1 und i_2 geschrieben.

Masche M1 (I): $i_1 \cdot R_1 + i_1 \cdot R_2 - i_2 \cdot R_2 = U_{01} - U_{02}$;

$i_1(R_1 + R_2) - i_2 \cdot R_2 = U_{01} - U_{02}$;

Masche M2 (II): $-i_1 \cdot R_2 + i_2 \cdot R_2 + i_2 \cdot R_3 = U_{02}$;

$-i_1 \cdot R_2 + i_2(R_2 + R_3) = U_{02}$;

IA) $i_1 \cdot 3 - i_2 \cdot 2 = 5$;

IIa) $-i_1 \cdot 2 + i_2 \cdot 7,6 = 5$; $/ \times 1,5$

IIb) $-i_1 \cdot 3 + i_2 \cdot 11,4 = 7,5$;

IA) + IIb): $i_2 \cdot 11,4 - i_2 \cdot 2 = 12,5$;

$i_2 \cdot 9,4 = 12,5 \Rightarrow i_2 = 1,33 \text{ [mA]}$

i_2 eingesetzt in IA): $i_1 \cdot 3 - 2,66 = 5 \Rightarrow i_1 = \frac{7,66}{3} = 2,55 \text{ [mA]}$

Es gilt: *) $I_1 = i_1$; $I_3 = i_2$

Knotenpunkt A: $I_2 = I_1 - I_3$ (da $i_1 > i_2$)

$I_2 = 2,55 \text{ mA} - 1,33 \text{ mA} = 1,22 \text{ mA}$;

Spannungsabfälle: $U_1 = I_1 \cdot R_1 = 2,55 \text{ mA} \cdot 1 \text{ k}\Omega = 2,55 \text{ V}$;

$U_2 = I_2 \cdot R_2 = 1,22 \text{ mA} \cdot 2 \text{ k}\Omega = 2,44 \text{ V}$;

$U_3 = I_3 \cdot R_3 = 1,33 \text{ mA} \cdot 5,6 \text{ k}\Omega = 7,45 \text{ V}$;

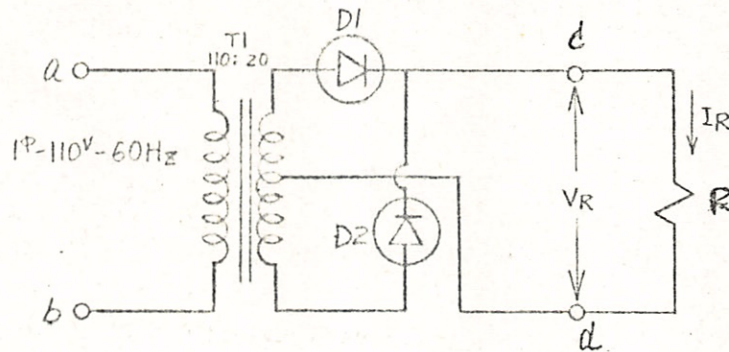
*) Anmerkung: Die Strompfeile I_2 und I_3 sind im Bild ent = sprechend den tatsächlichen Stromrichtungen umzukehren.

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Drawn			
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Page 2	XXIII. Internationaler Berufswettbewerb Fachtheorie (Fachrechnen)-Lösungsblatt		Industrie- Elektronik

16.

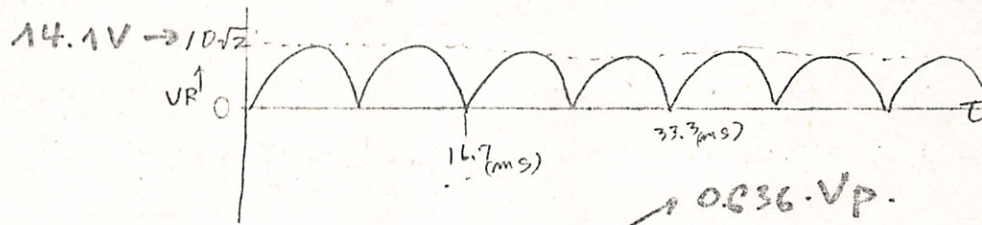
(2)



In the circuit in the figure above answer to the following questions, when the input voltage across a-b is 110V-60Hz sinusoidal wave and the ratio of the transformer T1 is 110:20.

訳
←

- (1) Sketch the wave form of the load voltage across the terminal c-d.



- (2) Calculate the average voltage V_R and average current I_R , assuming the forward voltage drop of the diodes (D1, D2) are zero and the value of the resistor (R) is 120-ohm.

$V_R =$ 9 (V) $I_R =$ 0.075 (A)

- (3) Determine the frequency of the current I_1 flowing through D1.

60 (Hz)

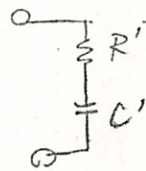
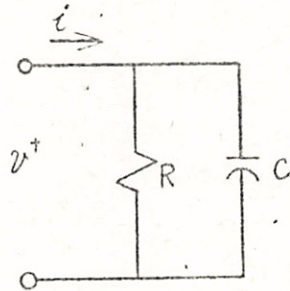
3. In the figure below, $R=5K\Omega$ and $C=0.5\mu F$.

Determine the two components of a series circuit having the same terminal admittance at $\omega=1000\text{rad/sec}$.

ASSUME THE PHASE SHIFT REMAINS EQUAL

図で $R=5k\Omega$, $C=0.5\mu F$ である。

$\omega=1000\text{rad/sec}$ の時 端子から見たアドミタンスが等しい 直列回路の2つの要素を求めよ。
但し移相は同じとして計算する。



$$X_C = \frac{1}{\omega C}$$

$$= \frac{1}{1000 \times 0.5 \times 10^{-6}}$$

$$= \frac{1}{5 \times 10^{-4}} [\Omega]$$

~~$$Z = \frac{1}{\frac{1}{R} + j\omega C}$$~~

$$Z = \frac{1}{j\omega C + \frac{1}{R}}$$

$$= \frac{1}{j5 \times 10^4 + \frac{1}{5 \times 10^3}}$$

$$= \frac{1}{j5 \times 10^{-4} + 2 \times 10^{-4}}$$

$$= \frac{10^4(2-j5)}{5^2+2^2}$$

$$= \frac{10^4(2-j5)}{29}$$

$$= 689.65 - j1724.1379$$

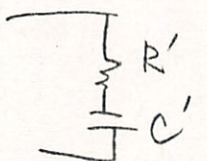
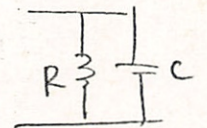
$$Z = \sqrt{\frac{1}{R^2}}$$

$$X_{C'} = \frac{1}{\omega C'}$$

$$= \frac{1}{\omega X_C'}$$

$$= \frac{1}{1000 \times 1724}$$

$$= 5.8 \times 10^{-7} [\mu F]$$



$$Z = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{R}{1 + (\omega CR)^2} - j \frac{\omega CR}{1 + (\omega CR)^2}$$

$$= R' - j \frac{1}{\omega C'}$$

$$\therefore R' = \frac{R}{1 + \omega^2 C^2 R^2} \quad C' = C \left(1 + \frac{1}{\omega^2 C^2 R^2} \right)$$

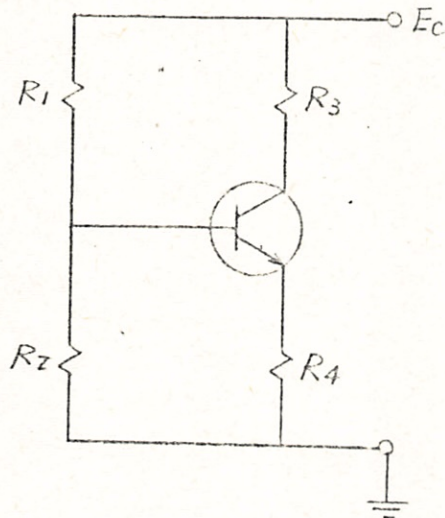
$$R' = 690 \Omega$$

$$C' = 0.58 \mu F$$

図のようなトランジスタ回路で、 $V_{BE} = 0.6\text{ V}$ 、 $I_B = 0$ の場合の
ベース電位 V_B 、コレクタ電位 V_C 、エミッタ電位 V_E および
コレクタ電流 I_C を求めよ

20. Given the transistor circuit of the figure below.

Calculate base voltage V_B , collector voltage V_C , emitter
voltage V_E and collector current I_C where $V_{BE} = 0.6\text{ V}$, $I_B = 0$.



$$E_C = 12\text{ V}$$

$$R_1 = 10\text{ k}\Omega$$

$$R_2 = 2\text{ k}\Omega$$

$$R_3 = 0.5\text{ k}\Omega$$

$$R_4 = 1\text{ k}\Omega$$

$$V_B = E_C \times \frac{R_2}{R_1 + R_2}$$

$$V_E = 12 \times \frac{2\text{ k}}{10\text{ k} + 2\text{ k}}$$

$$= 12 \times \frac{2}{12}$$

$$= 2\text{ V}$$

$$V_E = V_B - V_{BE}$$

$$= 2 - 0.6$$

$$= 1.4\text{ V}$$

$$I_C = I_E$$

$$= \frac{V_E}{R_4}$$

$$= \frac{1.4}{1\text{ k}}$$

$$= 1.4\text{ mA}$$

$$V_C = E_C - I_C \cdot R_3$$

$$= 12 - 1.4\text{ mA} \times 0.5\text{ k}$$

$$= 12 - 0.7$$

$$= 11.3\text{ V}$$

$$V_C = \boxed{11.3\text{ V}}$$

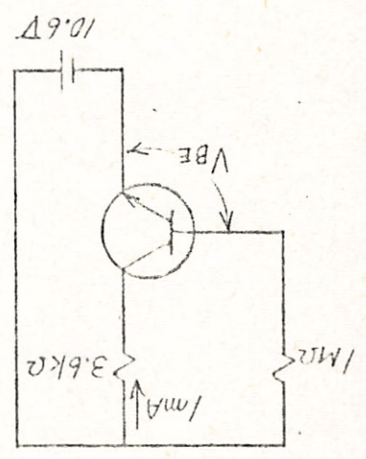
$$V_E = \boxed{1.4\text{ V}}$$

$$I_C = \boxed{1.4\text{ mA}}$$

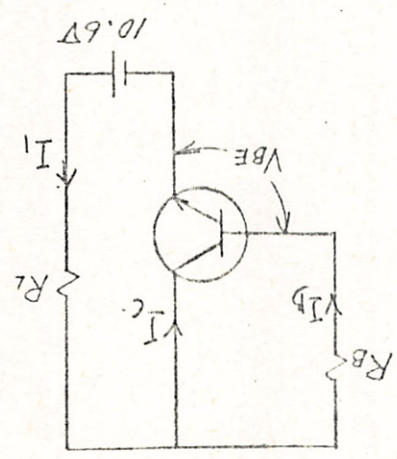
$$V_B = \boxed{2.0\text{ V}}$$

トランジスタの動作点か (a) 図 (b) 図で算出するたけには、
 $R_L \ll R_B$ といふことに注意せよ

18. Determine the R_L and R_B in figure (b) to get the same operating point as the biased circuit of figure (a).



(a)



(b)

$V_{BE} = 0.6V$

$$I_B = \frac{10.6 - V_{BE}}{1000}$$

$$= 0.01 \text{ mA}$$

$$I_C = 1 \text{ mA}$$

$$V_{CE} = 10.6 - 3.6 \times 1$$

$$= 7V$$

$$R_L = \frac{10.6 - 7}{I_C}$$

$$= \frac{3.6}{1.01}$$

$$= 3.57 \text{ k}\Omega$$

R_B

$$640 \text{ k}\Omega$$

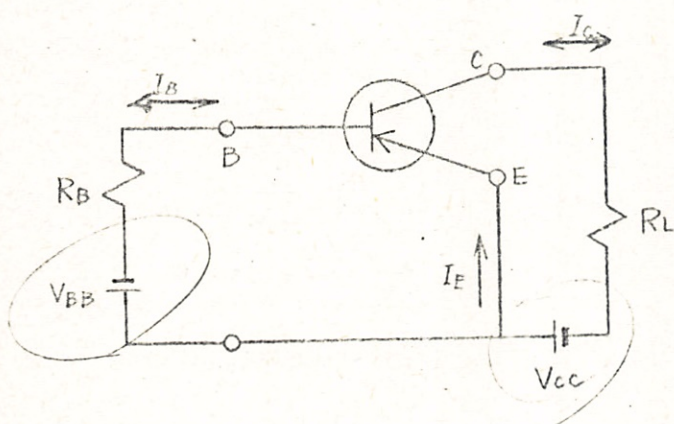
R_L

$$3.6 \text{ k}\Omega$$

4. 誤

11. A silicon PNP transistor is connected in the circuit shown below.

- (a) Complete the drawing by putting the arrowhead on the emitter electrode and by indicating the proper battery polarities, for a forward-biased emitter-base junction and a reverse-biased collector-base junction.
- (b) Assuming $|V_{BE}| = 0.7V$, calculate I_B for $V_{BB} = 6V$ and $R_B = 53K\Omega$.
- (c) If $V_{CC} = 12V$, $R_L = 2K\Omega$, and $\beta = 30$, calculate I_C , I_E , and V_{CE} .



$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$= \frac{6 - 0.7}{53}$$

$$= 0.1 \text{ (mA)}$$

$$I_C = \beta I_B$$

$$= 30 \times 0.01$$

$$= 3 \text{ (mA)}$$

$$I_B : +0.1 \text{ (mA)}$$

$$I_C : +3 \text{ (mA)}$$

$$I_E = I_B + I_C$$

$$= 3 + 0.1$$

$$= 3.1 \text{ (mA)}$$

$$V_{CE} = V_{CC} - I_C R_L$$

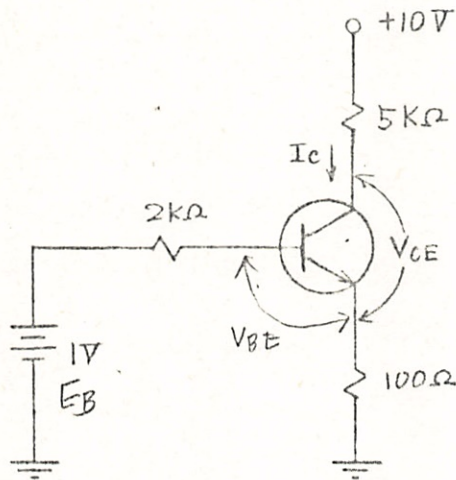
$$= 12 - 6$$

$$= 6$$

$$I_E : 3.1 \text{ (mA)}$$

$$V_{CE} : +6 \text{ (V)}$$

19. 図の回路において、 V_{CE} および I_C を求めよ。
 Given the circuit of the figure below.
 Calculate V_{CE} and I_C .



$$V_{BE} = 0.7V$$

$$\alpha = 0.9$$

$$I_{CBO} = 0$$

$$I_C = \frac{\alpha}{1-\alpha} I_B \quad \therefore I_B = \frac{1-\alpha}{\alpha} I_C$$

$$\begin{aligned} I_E &= I_C + I_B \\ &= I_C + \frac{1-\alpha}{\alpha} I_C \\ &= \frac{1}{\alpha} I_C \end{aligned}$$

$$I_B = \frac{E_B - V_{BE} - V_E}{R_B}$$

$$= \frac{E_B - V_{BE} - I_E R_E}{R_B}$$

I_B と I_E に I_C の式を代入

$$\frac{1-\alpha}{\alpha} I_C = \frac{E_B - V_{BE}}{R_B} - \frac{R_E}{R_B} \times \frac{1}{\alpha} I_C$$

$$\frac{1-\alpha}{\alpha} I_C + \frac{R_E}{R_B} \times \frac{1}{\alpha} I_C = \frac{E_B - V_{BE}}{R_B}$$

$$I_C \left(\frac{R_B(1-\alpha) + R_E}{\alpha R_B} \right) = \frac{E_B - V_{BE}}{R_B}$$

$$I_C = \frac{(E_B - V_{BE})\alpha}{R_B(1-\alpha) + R_E}$$

$$= \frac{(1-0.7) \times 0.9}{2k \cdot (1-0.9) + 0.1k}$$

$$= \frac{0.27}{0.3k} = 0.9 \text{ mA}$$

$$V_{CC} = R_C \times I_C + V_{CE} + R_E I_E$$

$$V_{CE} = V_{CC} - R_C \times I_C - R_E I_E$$

$$= V_{CC} - \left(R_C + \frac{R_E}{\alpha} \right) I_C$$

$$= 10 - \left(5k + \frac{0.1k}{0.9} \right) \times 0.9 \text{ mA}$$

$$= 10 - 4.5 - 0.1$$

$$= 5.4 \text{ (V)}$$

V_{CE} :

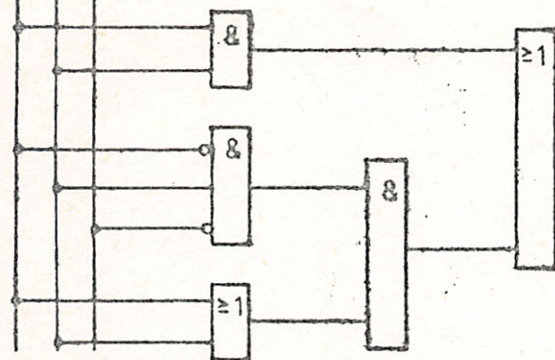
5.4 V

I_C :

0.90 mA

Aufgabe 3:

$X_1 X_2 X_3$



Überprüfen Sie, ob nebenstehende Schaltung vereinfacht werden kann. Wenn ja, geben Sie die einfachste Schaltung an.

3.1 bei Verwendung aller Grundgattertypen

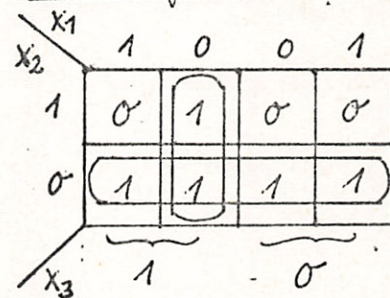
3.2 Aufbau nur mit NAND - Gattern

Lösung:

1. Aufstellen der Funktionstabelle

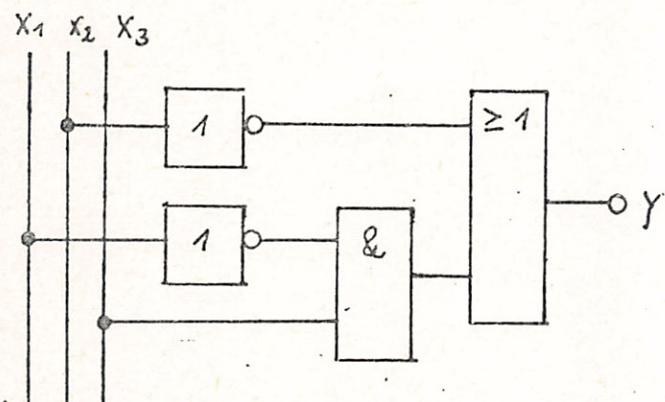
X_1	X_2	X_3	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

2. Einzeichnen der „1“en in das KV-Diagramm

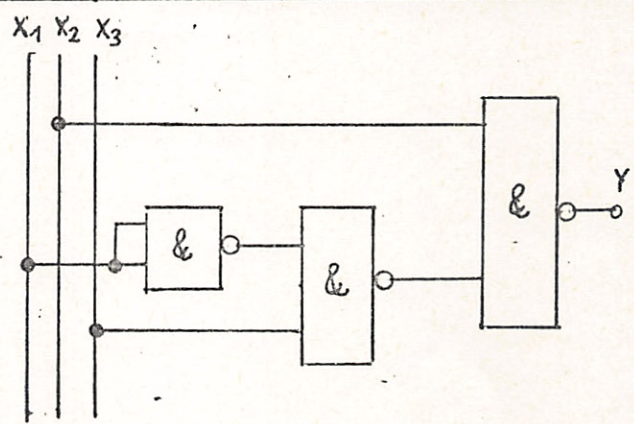


$$Y = \bar{X}_2 \vee \bar{X}_1 \wedge X_3$$

Vereinfachte Schaltung (Pkt. 3.1)



Schaltung nur mit NAND-Gattern (Pkt. 3.2)



PROPOSAL OF THE TECHNICAL REPRESENTATION OF GERMANY

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Page

XXIII. Internationaler Berufswettbewerb
Fachtheorie (Fachrechnen) - Lösungsblatt

Industrie-
Elektronik

← 訳 ①

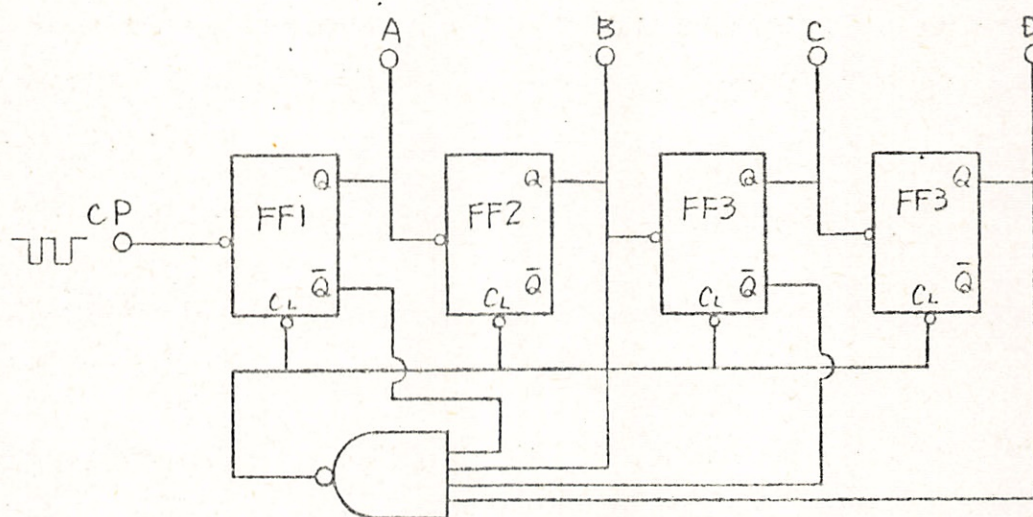
17. Given the IC(Integrated circuit) logic circuits shown in the figure below,

where, FF1, FF2, FF3, FF4 : Flip-flop ICs

CP : Input terminal of clock pulse

A, B, C, D : Output signal terminal.
(BCD cord output)

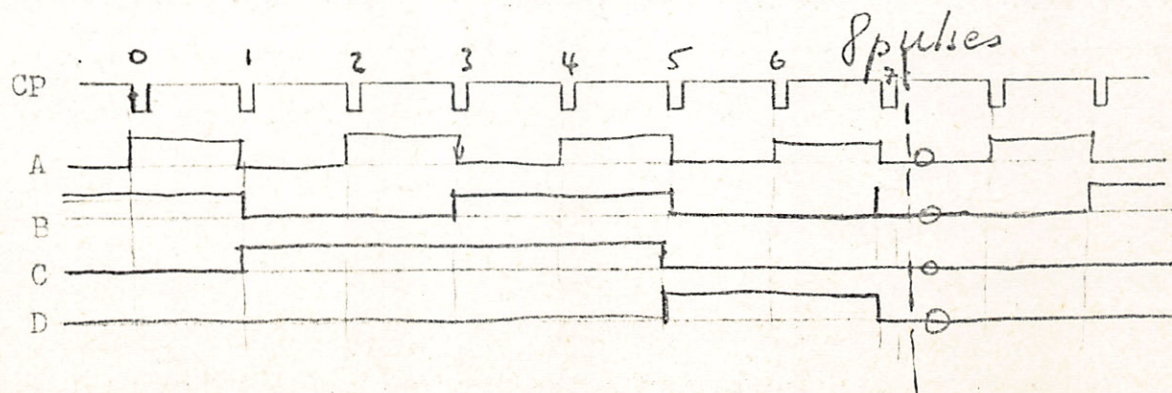
CL : Clear input when clear input is level '0', output Q is '0'.



(1) If the terminal B only is level "1" and others are level "0",
how many clock pulses make all output (A, B, C, D) levels
"0"?

8 個

(2) In the question (1), (where B is "1" and others are "0")
sketch the time charts of the output signals A, B, C, and D.



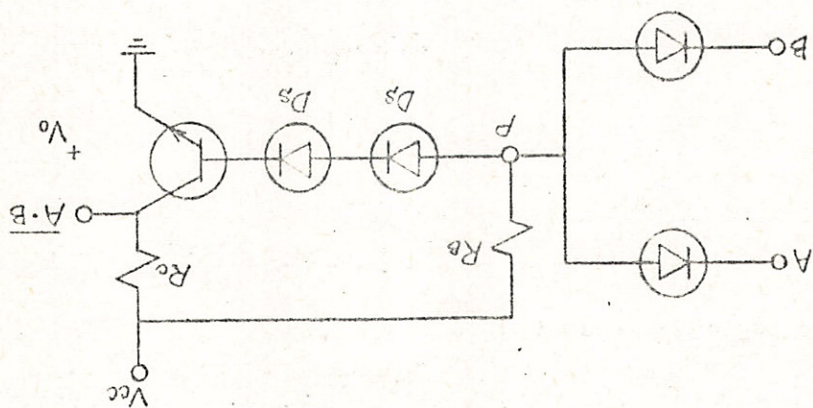
6. With the DTL NAND gate of the figure below, where, $V_{CC}=5V$, $R_E=R_C=5K\Omega$, $V_{DS}=0.7V$, and $\beta=30$, $V_{CE(sat)}=0.3V$, $V_{BE}=0.7V$ for the transistor.

(a) Determine the no-load output voltage, V_O , if input

$A=5V$ and $B=0.3V$.

(b) Determine the base current, collector and the no-load

output voltage, if input $A=5V$ and $B=2V$.



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$$V_o = 5[V]$$

$$I_B = 0.58[mA]$$

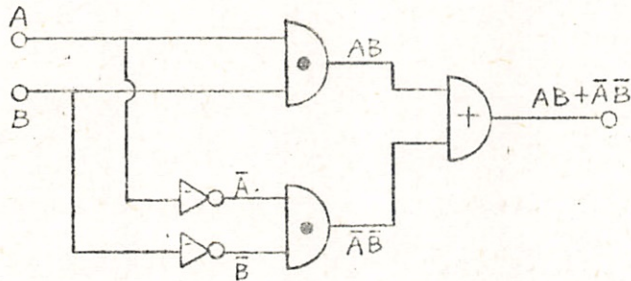
$$I_C = 0.94[mA]$$

$$V_o = 0.3[V]$$

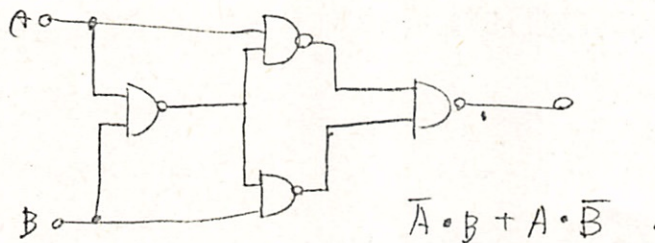


5. Show that the inverse of the inequality comparator is an "equality comparator" and synthesize a suitable circuit for it.

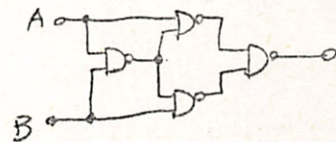
不一致回路の逆は 一致回路であることを証明し、
適当な回路を実現せよ。



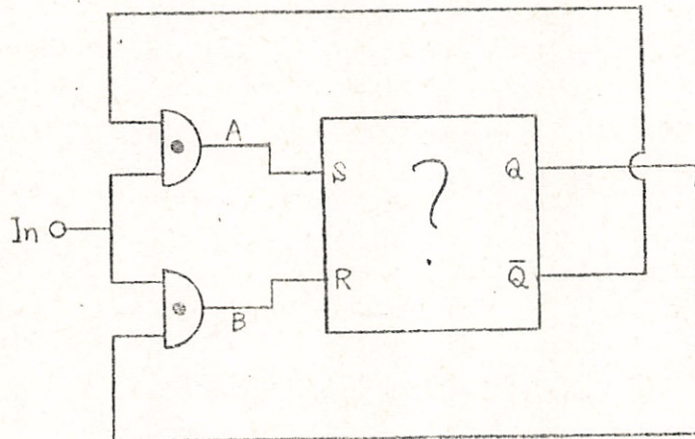
$$\overline{A \cdot B + A \cdot \bar{B}} = (A + \bar{B})(\bar{A} + B) = A \cdot B + \bar{A} \cdot \bar{B}$$



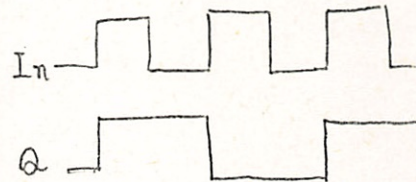
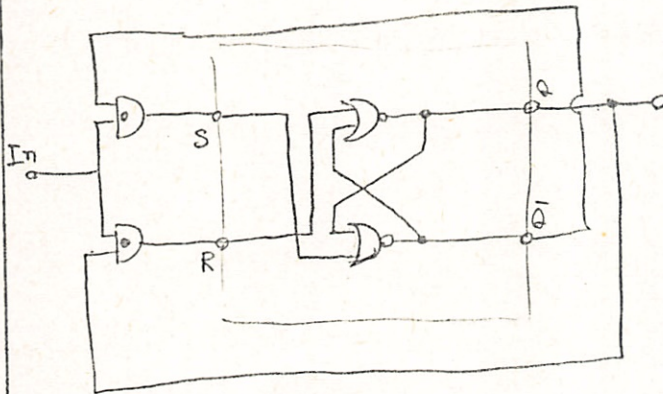
$$\overline{A \cdot B + A \cdot \bar{B}} = (A + \bar{B})(\bar{A} + B) = A \cdot B + \bar{A} \cdot \bar{B}$$



7. Analyze the memory element in the figure below.
 Draw up the truth table, assuming that the input is a series of pulses and that Q is initially 0.
~~What function is performed by the circuit?~~



下図のようにメモリーを含む回路で
 初期条件として $Q=0$ とし
 連続パルスを与えたときの
 真理値表を書け
 ANDゲートはどんな働きを
 持つ回路を構成するか？



In	0	1	0	1	0	1	0	1
Q	0	1	1	0	0	1	1	0

S, R に交互にパルスを入
 入る働きをする

9. The function, $f=A \cdot B$ is to be realized using only NOR gates.

Use DeMorgans theorems (to express f in terms of $C+D$ where C and D can be expressed in terms of A and B .)

Draw the necessary logic circuit and check by generating the truth table.

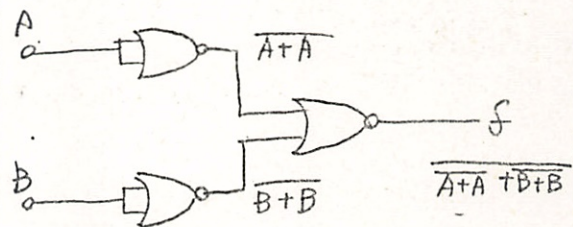
ドモルガンの法則を用いて $f = \overline{C+D}$ の形で表現せよ。

但し C, D は A と B で表わされる適当な論理回路を書け

そして真理値表を用いて確かめよ。

$$AB = \overline{\overline{A} + \overline{B}}$$

$$= \overline{A+A + B+B}$$



A	B	f
1	1	1
1	0	0
0	1	0
0	0	0

A	B	$\overline{A+A}$	$\overline{B+B}$	f
1	1	0	0	1
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0

②

10. Synthesize the following logic functions using NAND gates only:

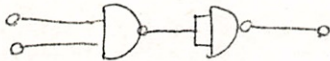
(a) AND, OR, NOR.

(b) Exclusive-OR.

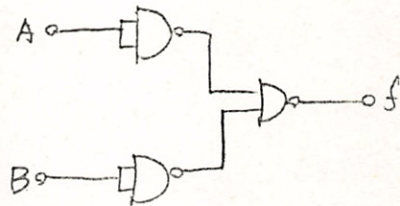
以下の (a)・(b) のロジック関数を
NANDゲートのみで表わせ

排他

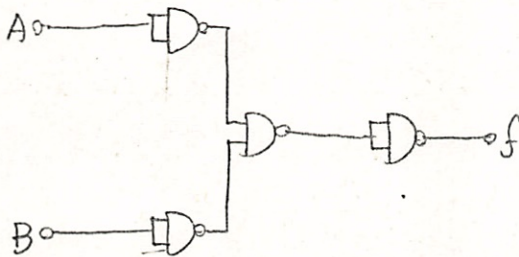
AND



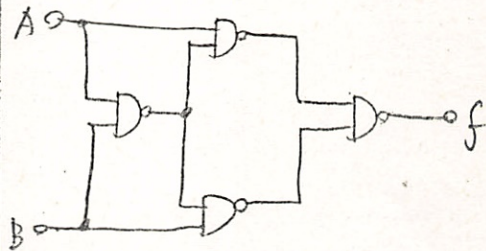
OR



NOR



Exclusive-OR



Aufgabe 7:

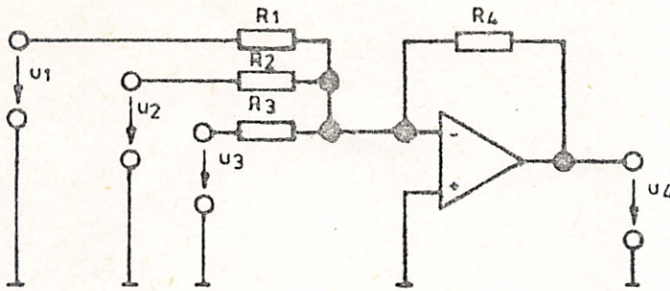
Wie groß ist die Ausgangsspannung u_a des im Bild dargestellten Addierers.

Gegeben:

$$u_1 = 1,8 \text{ V}; u_2 = 3,9 \text{ V}; u_3 = 4,3 \text{ V}$$

$$R_1 = 8,1 \text{ k}\Omega; R_2 = 12,0 \text{ k}\Omega;$$

$$R_3 = 15,0 \text{ k}\Omega; R_4 = 18,0 \text{ k}\Omega;$$



Lösung: Es handelt sich um einen Umkehraddierer, da das Signal dem invertierenden Eingang zugeführt wird.

$$\begin{aligned} u_a &= - \left(u_1 \frac{R_4}{R_1} + u_2 \frac{R_4}{R_2} + u_3 \frac{R_4}{R_3} \right) \\ &= - \left(1,8 \text{ V} \cdot \frac{18,0}{8,1} + 3,9 \text{ V} \cdot \frac{18,0}{12,0} + 4,3 \text{ V} \cdot \frac{18,0}{15,0} \right) \\ &= - (4,0 \text{ V} + 5,85 \text{ V} + 5,16 \text{ V}) = \underline{\underline{-15,01 \text{ V}}} \quad \checkmark \end{aligned}$$

DRAWING A PRINTED CIRCUIT BOARD DIAGRAM

Problem: Draw a parts placement/pattern diagram, using the data given below.

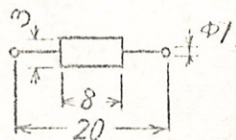
Working time limit: 1.5H

(1) Diagram drawing standard to follow

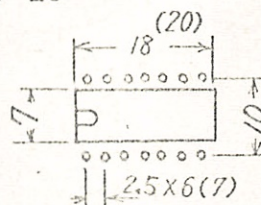
- A) The diagram should be a view seen from the pattern side. It is to be drawn in full lines.
- B) Parts placement and jumper lines are drawn in black with a pencil, and patterns in red with a pencil.
- C) Draw patterns on the grid or in straight lines at 45° .
- D) Give an insulating space of 1mm or more between patterns.
- E) Don't use a jumper wire so as possible.

(2) Outline and dimensions of parts

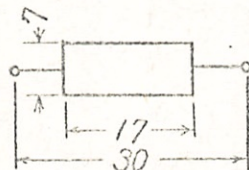
A) Resistance



D) IC

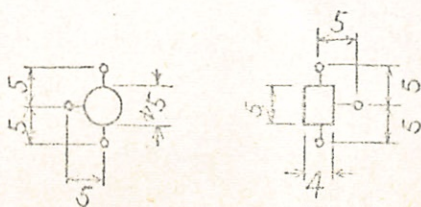


B) Condenser

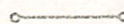


Numerals in (), parenthesis show dimensions in the case of using 16 pins.

C) Transistor

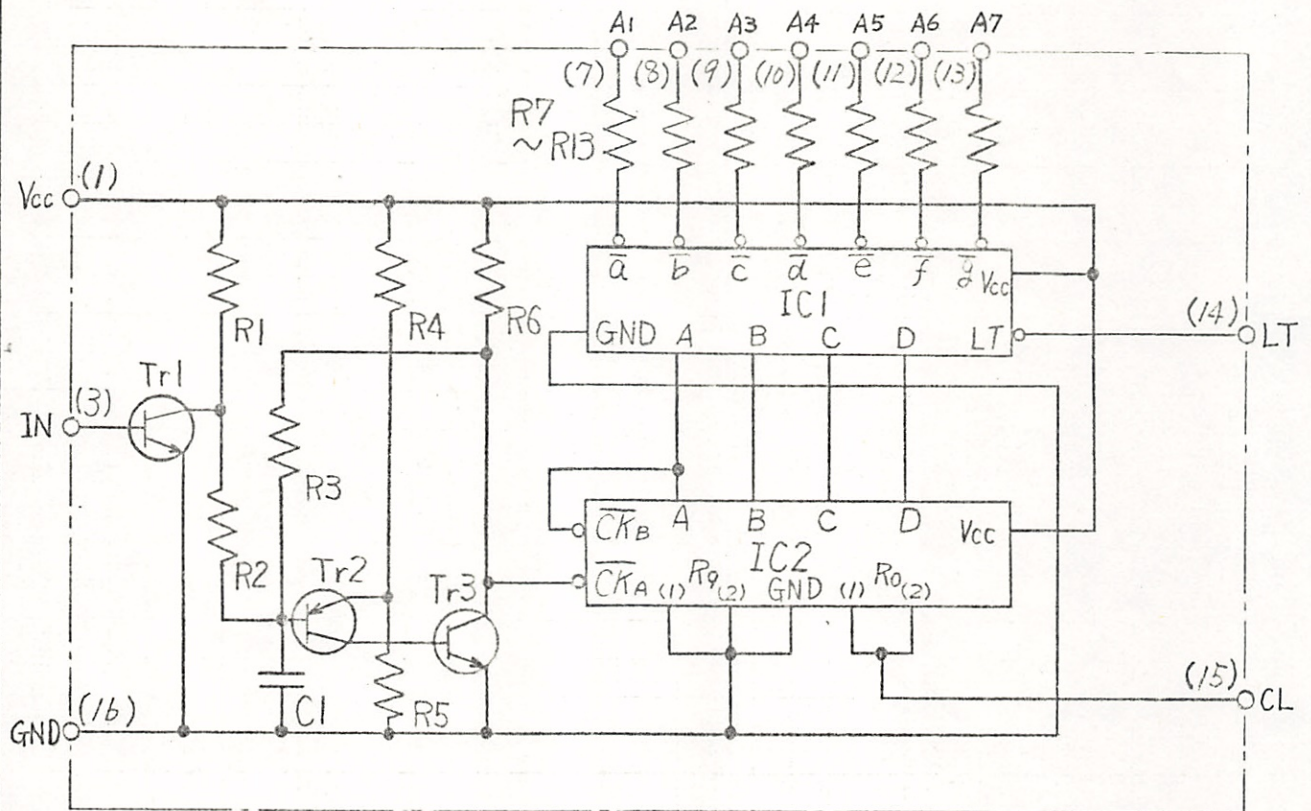


E) Jumper line



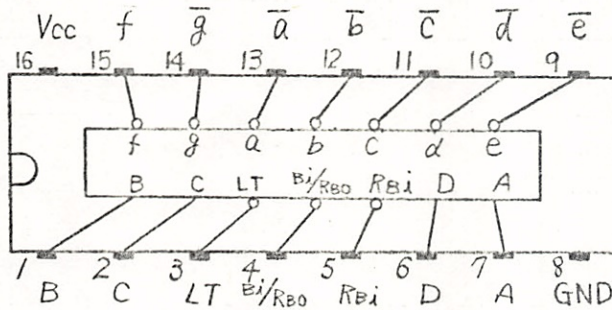
(3) Circuit diagram

Numerals in parenthesis, () show the terminal Nos, on the printed circuit board.

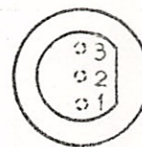


(4) Wiring of parts placed

A) IC1

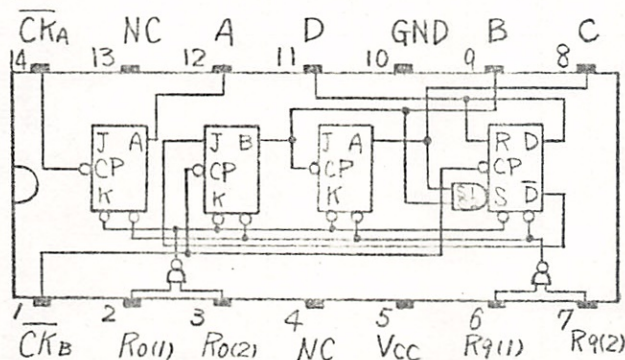


C) Tr1 . Tr3

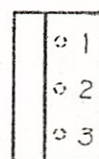


1. Emitter
2. Collector
3. Base

B) IC2



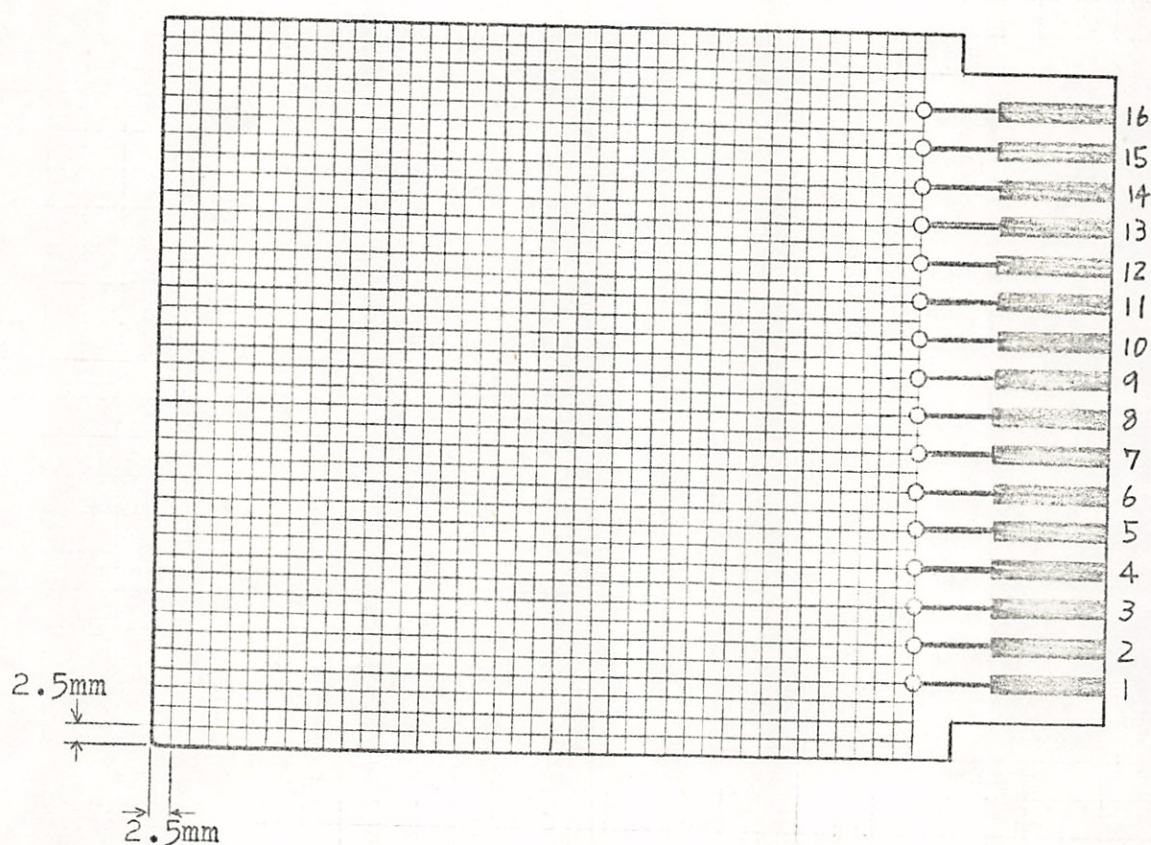
D) Tr2



1. Emitter
2. Collector
3. Base

(5) Diagram drawing paper

Pattern side



name: _____

Nationality: _____

DRAWING A PRINTED CIRCUIT BOARD DIAGRAM

Zeichnen Sie Bestückungsplan u. "Druck" eines Prints.
 Problem: Draw a parts placement/pattern diagram, using the data given below.

unter Verwendung der unten angegebenen Daten.

Working time limit: 1.5H

Arbeitszeit 75 Min.

Beachten Sie die folgenden Regeln:

(1) Diagram drawing standard to follow

A) The diagram should be a view seen from the pattern side. It is to be drawn in full lines.

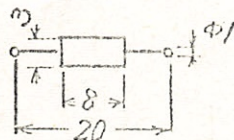
B) Parts placement and jumper lines are drawn in black. Die Bauteile u. die Drahtbrücken sind mit schwarzem Bleistift zu zeichnen, die Kupferverbindungen rot.
 Die Kupferverbindungen werden voll angezogen.

C) Draw patterns on the grid or in straight lines at 45°. Die Kupferverbindungen sind rechtwinklig und/oder unter 45° Winkel zu zeichnen.

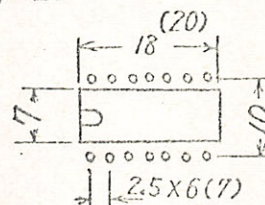
D) Give an insulating space of 1mm or more between patterns. Geben Sie zwischen den Kupferverbindungen 1mm Isolationsabstand oder mehr.

E) Don't use a jumper wire so as possible. Verwenden Sie möglichst wenig Drahtbrücken.
 Aussehen u. Abmessungen der Bauteile

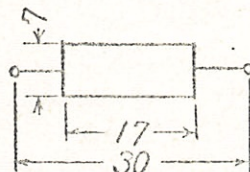
A) Resistance



D) IC

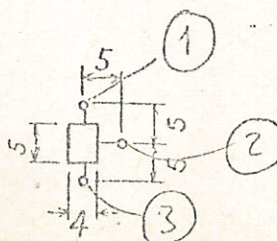
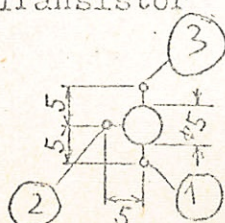


B) Condenser

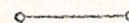


Die Zahlen in den Klammern gelten, Numerals in (), parenthesis, wenn 16, nicht 14 Kontaktstifte vorhanden werden
 or using 16 pins.

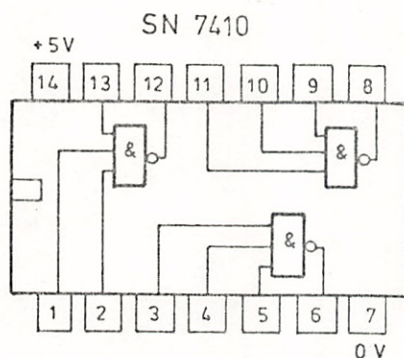
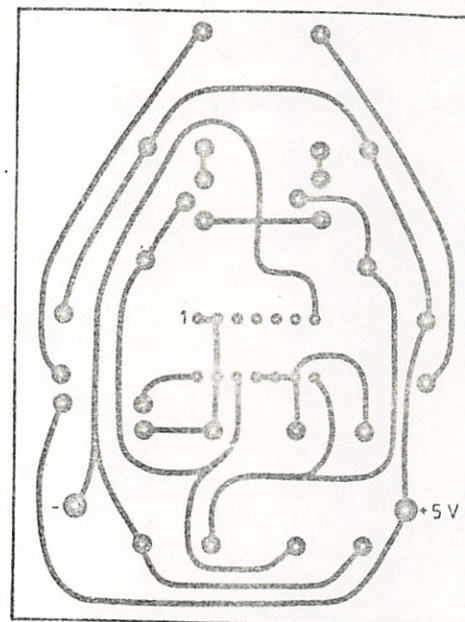
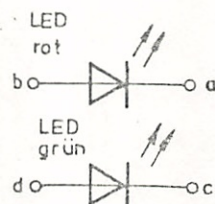
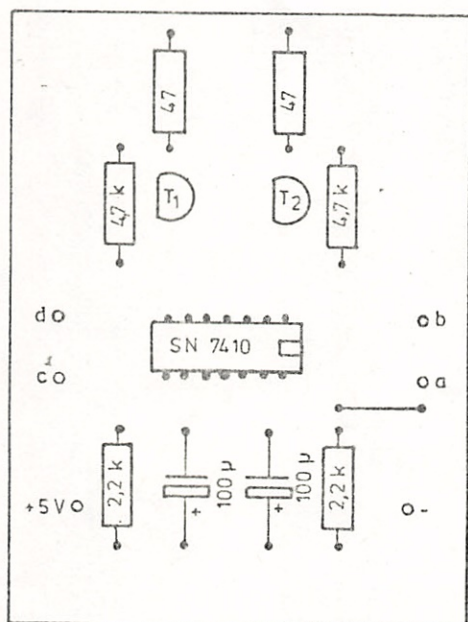
C) Transistor



E) Jumper line

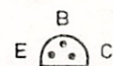


Entwerfen Sie aus Print und Bestückungsplan den dazu
gehörenden Stromlaufplan .



BC 308

T1/T2



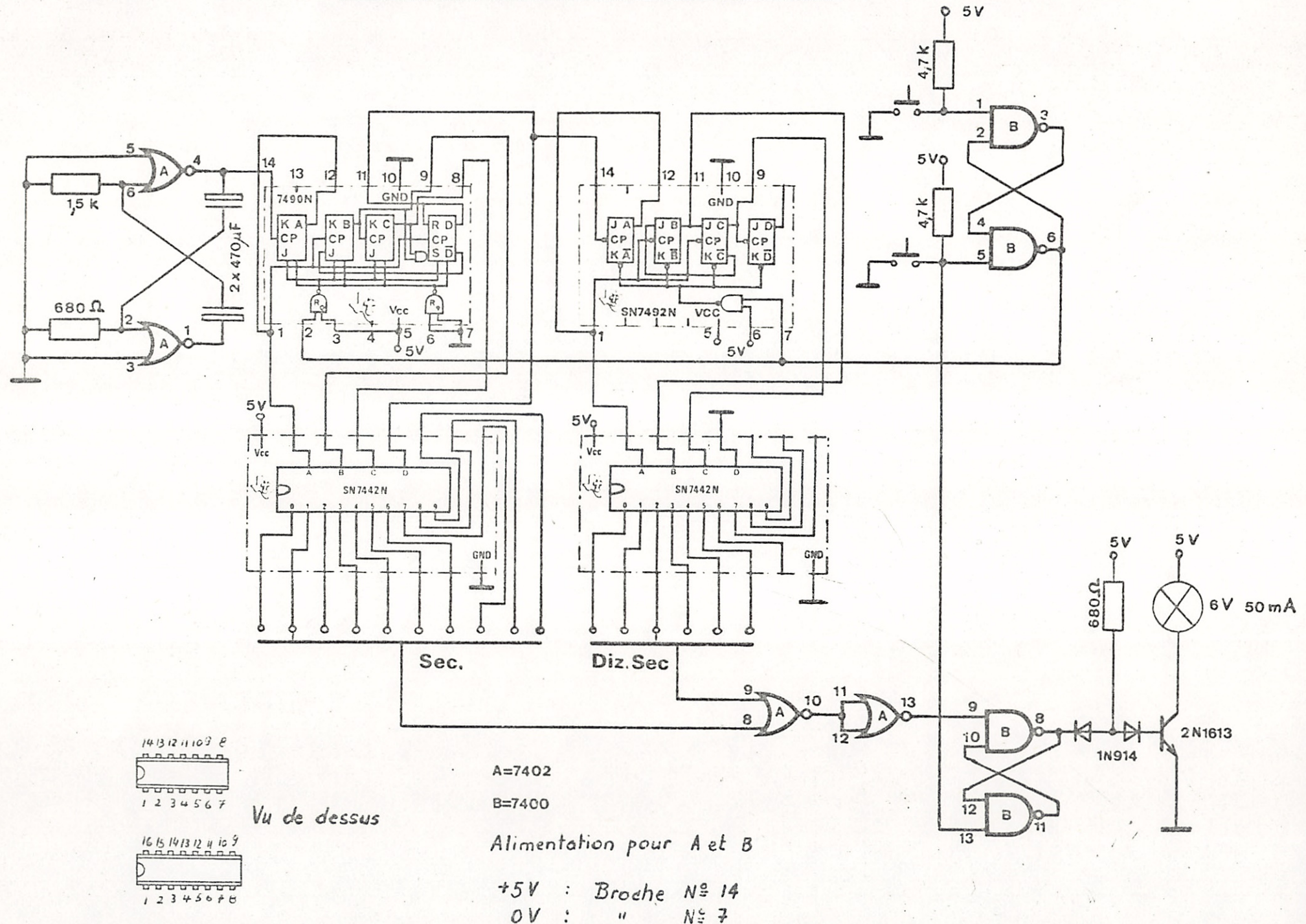
Lösung :

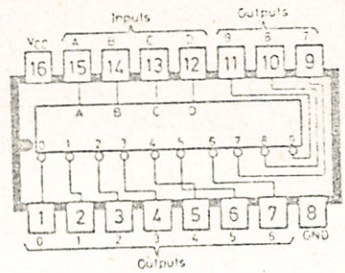
PROPOSAL OF THE TECHNICAL REPRESENTATION OF GERMANY

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Drawn		
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MINUTERIE PROGRAMMABLE 0 - 59s



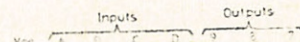


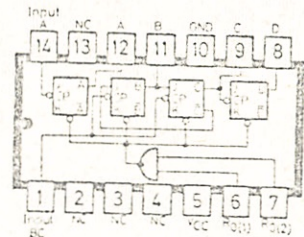
- TTL Ein- und Ausgänge
- Eingangskapazitäten
- Aktiver Ausgang im "L"-Zustand
- Stiftbelegung gleich mit den Typen SN7445/145N
- Typ. Impulsverzögerungszeit 22 ns
- Typ. Leistungsaufnahme 140 mW

Wahrheitstabelle
SN5442/SN7442

BCD Input				All Types decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	H	L	H	H	H	H	L	H	H	H	H	H
L	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	L	H	H	H	H	H	H	H	H	L	H	H
H	L	H	L	H	H	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	H	L	H	H	H	H	H	H	H	H	H	L
H	H	H	H	H	H	H	H	H	H	H	H	H	L

	Meßpunkt	Zustand	Eingang	Ausgang
Last-Faktoren	Eingänge		1,0	
	Ausgänge			10,0
SN7442N SN5442N SN8442N		BCD-zu-Dezimal-Dekoder		





- TTL Ein- und Ausgänge
- Eingangskapazitäten
- Negativ flankengesteuert
- Max. Zählfrequenz 10 MHz
- Min. Taktimpulsbreite 50 ns
- Typ. Leistungsaufnahme 155 mW

Wahrheitstabelle
(See Notes 1, 2 and 3)

Count	Output			
	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

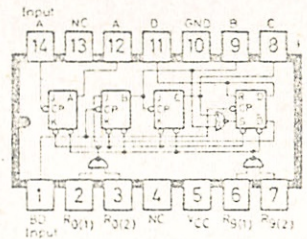
Notes:

1. Output A connected to input B
2. To reset all outputs to logical 0 both R0(1) and R0(2) inputs must be at logical 1.
3. Either (or both) reset inputs R0(1) and R0(2) must be at a logical 0 to count.

	Meßpunkt	Zustand	Eingang	Ausgang
Last-Faktoren	R0(1) und R0(2) Eingänge	L	1,0	
	B/C Eingang	L	4,0	
	A Eingang	L	2,0	
	Ausgänge	L		10,0

SN7492N
SN5492N
SN8492N

Teiler durch 12

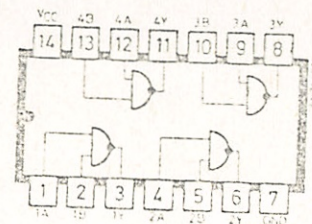


- TTL Ein- und Ausgänge
- Eingangskapdiolen
- Negativ flankengetriggert
- Max. Zehlfrequenz 25 MHz
- Min. Taktimpulsbreite 50 ns
- Typ. Leistungsaufnahme 160 mW

Wahrheitstabelle
Reset/Count

Reset inputs				output			
R0(1)	R0(2)	R1(1)	R1(2)	D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

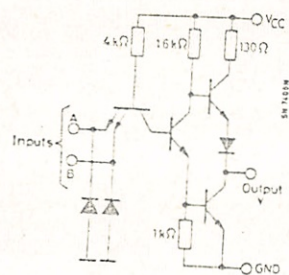
	Meßpunkt	Zustand	Eingang	Ausgang
Last-Faktoren	A-Eingang	L	2,0	
	BD-Eingang	L	4,0	
	Alle anderen Eingänge	L	1,0	
	Ausgänge	L *		10,0
SN7490N-S1		Dezimalzähler		



positive logic $Y = \overline{AB}$

- TTL Ein- und Ausgänge
- Eingangskapdioden
- Impulsverzögerungszeit 10 ns
- Typ. Leistungsaufnahme 40 mW

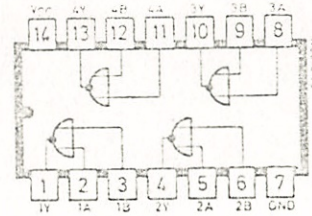
Schematik



	Meßpunkt	Zustand	Eingang	Ausgang
Last-Faktoren	Eingänge	L	1.0	
	Ausgänge	L		10.0

SN7400N
SN5400N
SN6400N

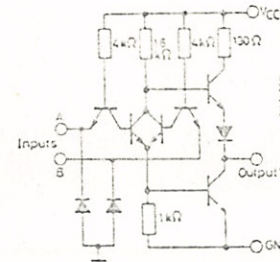
Vierfaches NAND-Gatter
mit je zwei Eingängen



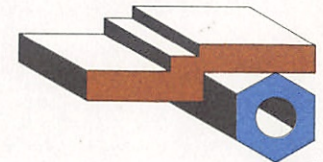
positive logic: $Y = A + B$

- TTL Ein- und Ausgänge
- Eingangskapazitäten
- Max. zulässige Ausgangsspannung 5,5 V/250 μ A
- S1-Selektion:
Max. zulässige Ausgangsspannung 5,5 V/500 μ A
- Typ. Impulsverzögerungszeit 10 ns
- Typ. Leistungsaufnahme 48 mW

Schematik



	Messpunkt	Zustand	Eingang	Ausgang
Last-Faktoren	Eingänge	L	1,0	
	Ausgänge	L		10,0
SN7402N SN7402N-S1 SN5402N SN5402N-S1 SN8402N		Viertaches NOR-Gatter mit je zwei Eingängen		



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